What is claimed is:

1. A shift register in which multiple stages are connected one after another to each other, the multiple stage having a first stage in which a start signal is coupled to an input terminal, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd stages for receiving a first clock signal and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

each of the multiple stages comprising:

a pull-up means for providing a corresponding one of the first and second clock signals to an output terminal;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal and turning off the pull-up means in response to a front edge of an output signal of a next stage;

a pull-down means for providing a first power voltage to the output terminal; and

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to the front edge of the input signal and turning on the pull-down means in response to the front edge of the output signal of the next stage.

2. The shift register of claim 1, wherein each of the multiple stages further comprises a floating preventing means connected to the input node of the pull-down means, wherein the floating preventing means provides a second power

voltage to the input node of the pull-down means to prevent the input node of the pull-down means from being floated.

3. The shift register of claim 2, wherein each of the multiple stages further comprises a turn-on preventing means connected to the input node of the pull-down means, wherein the turn-on preventing means provides the first power voltage to the input node of the pull-down means in response to the output signal of the output terminal to prevent the pull-down means from being turned on.

4. The shift register of claim 3, wherein the turn-on preventing means comprises an NMOS transistor of which drain is connected to the input node of the pull-down means, gate is connected to the output terminal and source is connected to the first power voltage.

5. The shift register of claim 2, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain and gate are commonly connected to the input terminal and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is

connected to the first power voltage.

6. The shift register of claim 5, wherein the pull-down driving means comprises:

a fourth transistor of which drain is connected to the second power voltage, gate is connected to the output signal of the next stage and source is connected to the input node of the pull-down means; and

a fifth transistor of which drain is connected to the input node of the pull-down means, gate is connected to the input signal and source is connected to the first power voltage.

7. The shift register of claim 6, wherein the floating preventing means comprises a sixth transistor of which drain and gate are connected to the second power voltage and source is connected to the input node of the pull-down means, wherein the sixth transistor has a size smaller sufficiently than the fifth transistor.

8. The shift register of claim 7, wherein a size ratio of the fifth transistor to the sixth transistor is approximately 20:1.

9. An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages connected one after another to each other, the multiple stages having a first stage in

which a start signal is coupled to an input terminal, for sequentially selecting the multiple gate lines using an output signal of each stage, and the multiple stages having odd stages for receiving a first clock signal, and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

wherein the each stage comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a corresponding gate line;

a control terminal connected to an output terminal of a next stage;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up means connected between the clock terminal and the output terminal, for pulling-up the corresponding gate line during a duty period of the clock signal of when the pull-up means is turned on;

a pull-down means connected between the output terminal and a first power voltage, for pulling-down the corresponding gate line when the pull-down means is turned on;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up means in response to a front edge of a control signal supplied to the control terminal;

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to the front edge of the input signal and turning on the pull-down means in response to the front edge of the control signal; and

a floating preventing means connected between the input node of the pull-down means and a second power voltage, for always connecting the second

power voltage to the input node of the pull-down means to prevent the input node of the pull-down means from being floated.

10. The LCD of claim 9, wherein each of the multiple stages further comprises a turn-on preventing means connected between the input node of the pull-down means and the first power voltage, wherein the turn-on preventing means connects the first power voltage to the input node of the full down means in response to the output signal of the output terminal to prevent the pull-down means from being turned on.

11. The LCD of claim 10, wherein the turn-on preventing means comprises an NMOS transistor of which drain is connected to the input node of the pull-down means, gate is connected to the output terminal and source is connected to the first power voltage.

12. The LCD of claim 11, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain and gate are commonly connected to the input terminal and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the control terminal and source is connected to the first

power voltage.

13. The LCD of claim 12, wherein the pull-down driving means comprises:

a fourth transistor of which drain is connected to the second power voltage, gate is connected to the control terminal and source is connected to the input node of the pull-down means; and

a fifth transistor of which drain is connected to the input node of the pull-down means, gate is connected to the input terminal and source is connected to the first power voltage.

14. The LCD of claim 13, wherein the floating preventing means comprises a sixth transistor of which drain and gate are connected to the second power voltage and source is connected to the input node of the pull-down means, wherein the sixth transistor has a size smaller than the fifth transistor.

15. The LCD of claim 14, wherein a size ratio of the fifth transistor to the sixth transistor is approximately 20:1.

16. The LCD of claim 9, further comprising an external connection terminal having five terminals of a first clock signal input terminal, a second clock signal input terminal, a start signal input terminal, a first power voltage input terminal and a second power voltage input terminal.

17. The LCD of claim 9, wherein each of the display cell array circuit,

the data driving circuit and the gate driving circuit is of an NMOS transistor made of amorphous silicon TFT.

18. An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line,

wherein the data driving circuit comprises multiple data line blocks and a shift register,

wherein each of the data line blocks comprises multiple driving transistors each of which drain and source are respectively connected between a data input terminal and the data line and gate is commonly connected to a block selection terminal,

wherein the shift register comprises multiple stages connected one after another to each other, the multiple stages having a first stage in which a block selection start signal is coupled to an input terminal, for sequentially selecting the multiple data line blocks using an output signal of each stage, and the multiple stages consisting of odd stages for receiving a first clock signal; and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

wherein each stage comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a block selection terminal of a corresponding data line block;

a control terminal connected to an output terminal of a next stage;

a clock terminal into which a corresponding clock signal is input;

a pull-up means connected between the clock terminal and the output terminal, for pulling-up the corresponding gate line during a duty period of the clock signal of when the pull-up means is turned on;

a pull-down means connected between the output terminal and a first power voltage, for pulling-down the corresponding gate line using the first power voltage when the pull-down means is turned on;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up means in response to a front edge of a control signal supplied to the control terminal; and

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to the front edge of the input signal and turning on the pull-down means in response to the front edge of the control signal.

19. The LCD of claim 18, wherein said each stage comprises a floating preventing means connected between the input node of the pull-down means and a second power voltage, the input node of the pull-down means being always connected to the second power voltage, for preventing the input node of the pull-down means from being floated.

20. The LCD of claim 19, wherein said each stage further comprises a turn-on preventing means connected between the input node of the pull-down means and the first power voltage, wherein the turn-on preventing means connects the first power voltage to the input node of the pull-down means in response to the output

signal of the output terminal to prevent the pull-down means from being turned.

21. The LCD of claim 20, wherein the turn-on preventing means comprises an NMOS transistor of which drain is connected to the input node of the pull-down means, gate is connected to the output terminal and source is connected to the first power voltage.

22. The LCD of claim 21, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain and gate are commonly connected to the input terminal and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the control terminal and source is connected to the first power voltage.

23. The LCD of claim 22, wherein the pull-down driving means comprises:

a fourth transistor of which drain is connected to the second power voltage, gate is connected to the control terminal and source is connected to the input node of the pull-down means; and

a fifth transistor of which drain is connected to the input node of the pull-down

means, gate is connected to the input terminal and source is connected to the first power voltage.

24. The LCD of claim 23, wherein the floating preventing means comprises a sixth transistor of which drain and gate are connected to the second power voltage and source is connected to the input node of the pull-down means, wherein the sixth transistor has a size smaller than the fifth transistor.

25. The LCD of claim 24, wherein a size ratio of the fifth transistor to the sixth transistor is approximately 20:1.

26. The LCD of claim 18, further comprising an external connection terminal having a first clock signal input terminal, a second clock signal input terminal, a block selection start signal input terminal and multiple data input terminals.

27. The LCD of claim 18, wherein each of the display cell array circuit, the data driving circuit and the gate driving circuit comprises a NMOS transistor made of amorphous silicon TFT.

28. An LCD having an LCD module in which a liquid crystal is interposed between a lower transparent substrate and an upper transparent substrate, the LCD comprising:

a display cell array circuit formed on the lower transparent substrate, comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line,

a gate driving circuit formed on the lower transparent substrate and comprising a first shift register comprising multiple stages connected one after another to each other, the multiple stages having a first stage in which a start signal is coupled to an input terminal, the first shift register sequentially selecting the multiple gate lines using an output signal of each stage;

a data driving circuit formed on the lower transparent substrate and comprising multiple data line blocks and a second shift register, each of the data line blocks comprising multiple driving transistors each of which drain and source are connected between a data input terminal and the data line and gate is commonly connected to a block selection terminal, the second shift register comprising multiple stages connected one after another to each other, the multiple stages having a first stage in which a block selection start signal is coupled to an input terminal, for sequentially selecting the multiple data line blocks using an output signal of each stage; and

a flexible PCB on which an integral control and data driving chip is mounted, for providing a control signal and a data signal to the input terminal of the gate and data driving circuits.

29. The LCD of claim 28, wherein the multiple stages of each of the first and second shift registers consist of odd stages for receiving a first clock signal; and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

wherein each stage comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a corresponding gate line or data line block;

a control terminal connected to an output terminal of a next stage;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up means connected between the clock terminal and the output terminal, for pulling-up the output terminal during a duty period of the clock signal of when the pull-up means is turned on;

a pull-down means connected between the output terminal and a first power voltage, for pulling-down the corresponding gate line when the pull-down means is turned on;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up means in response to a front edge of a control signal supplied to the control terminal;

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to a front edge of the input signal and turning on the pull-down means in response to the front edge of the control signal; and

a floating preventing means connected between the input node of the pull-down means and a second power voltage, for always connecting the second power voltage to the input node of the pull-down means to prevent the input node of the pull-down means from being floated.

30. The LCD of claim 28, wherein a duty period of the first and second clock signals applied to the first shift register is greater than a period of a duty period of the first and second clock signals applied to the second shift register multiplied by a number of the data line blocks.

31. The LCD of claim 28, wherein the lower transparent substrate is connected to the flexible PCB through an external connection terminal, wherein the external connection terminal comprises: five terminals connected to the data driving circuit of a first clock signal input terminal, second clock signal input terminal, scan start signal input terminal, first power voltage input terminal and second power voltage input terminal; and three control terminals of first clock signal input terminal, second clock signal input terminal and block selection start signal input terminal and multiple data input terminals all of which are connected to the data driving circuit.

32. A shift register in which multiple stages are connected one after another to each other, the multiple stage having a first stage in which a start signal is inputted into an input terminal, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd stages for receiving a first clock signal and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

each of the multiple stages comprising:

a pull-up means for providing a corresponding one of the first and second clock signals to an output terminal;

a pull-up driving means, connected to an input node of the pull-up means, for charging a capacitor in response to a front edge of an input signal to turn on the pull-up means and discharging the capacitor in response to a front edge of an output signal of a next stage to turn off the pull-up means;

a pull-down means for providing a first power voltage to the output terminal; and

a pull-down driving means, connected to an input node of the pull-down means and the input node of the pull-up means, for turning off the pull-down means and turning on the pull-down means in response to the front edge of the output signal of the next stage.

33. The shift register of claim 32, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain is connected to the input node of the pull-up means, gate is connected to an output signal of a next stage and source is connected to the first power voltage;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage.

34. The shift register of claim 33, wherein a size ratio of the first transistor to the second transistor is approximately 2:1.

35. The shift register of claim 33, wherein the pull-down driving means comprises:

a fourth transistor of which drain and gate are commonly connected to the

second power voltage and source is connected to the input node of the pull-down means; and

a fifth transistor of which drain is connected to the input node of the pull-down means, gate is connected to the input node of the pull-up means and source is connected to the first power voltage.

36. The shift register of claim 35, wherein a size ratio of the third transistor to the fifth transistor is approximately 16:1.

37. The shift register of claim 32, further comprising an external connection terminal having five terminals of a first clock signal input terminal, a second clock signal input terminal, a start signal input terminal, a first power voltage input terminal and a second power voltage input terminal.

38. The shift register of claim 32, wherein a phase difference is placed between high level periods of the first and second clock signals.

39. A shift register in which multiple stages are connected one after another to each other, the multiple stage having a first stage in which a start signal is inputted into an input terminal, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd stages for receiving a first clock signal and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

each of the multiple stages comprising:

an NMOS pull-up transistor of which drain is connected to a corresponding

clock signal, gate is connected to a first node and source is connected to an output terminal;

an NMOS pull-down transistor of which drain is connected to the output terminal, gate is connected to a second node and source is connected to a first power voltage;

a capacitor connected between the first node and the output terminal;

a first transistor of which drain is connected to a second power voltage, gate is connected to an input signal and source is connected to the first node;

a second transistor of which drain is connected to the first node, gate is connected to an output signal of a next stage and source is connected to the first power voltage;

a third transistor of which drain is connected to the first node, gate is connected to the second node and source is connected to the first power voltage;

a fourth transistor of which drain and gate are commonly connected to the second power voltage and source is connected to the second node; and

a fifth transistor of which drain is connected to the second node, gate is connected to the first node and source is connected to the first power voltage.

40. The shift register of claim 39, wherein a size ratio of the first transistor to the third transistor is approximately 2:1.

41. The shift register of claim 39, wherein a size ratio of the fourth transistor to the fifth transistor is approximately 16:1.

42. The shift register of claim 39, wherein each of the transistors is of an

NMOS transistor made of amorphous silicon TFT.

43. A shift register including multiple stages connected in a cascade fashion, the multiple stages having a first stage in which a start signal is coupled to an input terminal, for sequentially outputting output signals of the respective stages, the multiple stages having odd stages for receiving a first clock signal and a second clock signal having a phase opposite to the first clock signal at a first clock terminal and a second clock terminal of the odd stages, and even stages for receiving the second clock signal and the first clock signal at a first clock termianl and a second clock terminal of the even stages,

wherein each of the multiple stages comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a corresponding gate line;

a first control terminal connected to a second control terminal of a stage after a next stage;

a second control terminal;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up means for providing a corresponding one out of the first and second clock signals to the output terminal;

a pull-down means for providing a first power voltage to the output terminal;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal and turning off the pull-up means in response to a front edge of a control signal supplied to the control terminal; and

a pull-down driving means connected to an input node of the pull-down

means and an input node of the pull-up means, for turning off the pull-down means, and for turning on the pull-down means in response to a front edge of an output signal of the next stage.

44. The shift register of claim 43, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain and gate are commonly connected to the input signal and source is connected to the input node of the pull-up means; and

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is connected to the first power voltage.

45. The shift register of claim 44, wherein the first transistor receives the start signal or the input signal from the previous stage through the commonly connected gate and drain, and charges the capacitor through a source thereof.

46. The shift register of claim 44, wherein the pull-up driving means discharges the control signal of the pull-up means using a pull-up control signal provided from the second control terminal.

47. The shift register of claim 43, wherein the pull-down driving means comprises:

a third transistor of which drain is connected to the first power voltage, gate is

connected to the output signal of the next stage and source is connected to the input node of the pull-down means; and

a fourth transistor of which drain and gate are commonly connected to the second clock signal and source is connected to the input node of the pull-down means.

48. An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages connected in a cascade fashion, the multiple stages having a first stage in which a start signal is coupled to an input terminal, the shift register for sequentially outputting output signals of the respective stages, the multiple stages having odd stages for receiving a first clock signal and a second clock signal having a phase opposite to the first clock signal at a first clock terminal and a second clock terminal of the odd stages, and even stages for receiving the second clock signal and the first clock signal at a first clock termianl and a second clock terminal of the even stages,

wherein each of the multiple stage comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a corresponding gate line;

a first control terminal connected to a second control terminal of a stage after a next stage;

a second control terminal;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up means connected between the clock terminal and the output terminal, for turning on the corresponding gate line during a duty period of the clock signal;

a pull-down means connected between the output terminal and a first power voltage, for pulling-down the corresponding gate line when the pull-down means is turned on;

a pull-up driving means connected to an input node of the pull-up means, for turning on the pull-up means in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up means in response to a front edge of a control signal of the stage after the next stage supplied to the control terminal; and

a pull-down driving means connected to an input node of the pull-down means and an input node of the pull-up means, for turning off the pull-down means and for turning on the pull-down means in response to a front edge of an output signal of the next stage.

49. The LCD of claim 48, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which drain and gate are commonly connected to the input signal and source is connected to the input node of the pull-up means; and

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is connected to the first power voltage.

50. The LCD of claim 49, wherein the first transistor receives the start

signal or the input signal from the previous stage through the commonly connected gate and drain, and charges the capacitor through a source thereof.

51. The LCD of claim 48, wherein the pull-up driving means discharges the control signal of the pull-up means using a pull-up control signal provided from the second control terminal of the stage after the next stage.

52. The LCD of claim 48, wherein the pull-down driving means comprises:

a third transistor of which drain is connected to the first power voltage, gate is connected to the output signal of the next stage and source is connected to the input node of the pull-down means; and

a fourth transistor of which drain and gate are commonly connected to the second clock signal and source is connected to the input node of the pull-down means.

53. A shift register including multiple stages connected in a cascade fashion, the multiple stages having a first stage in which a start signal is coupled to an input terminal, for sequentially outputting output signals of the respective stages, the multiple stages including odd stages for receiving a first clock signal and a second clock signal having a phase opposite to the first clock signal,

wherein each of the multiple stages comprises:

a pull-up means for providing a corresponding one out of the first and second clock signals;

a pull-down means for providing a first power voltage to the output terminal;

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to a front edge of the input signal and turning on the pull-down means in response to a front edge of an output signal of a next stage; and

a pull-up driving means provided with a capacitor of which a first end is connected to an input node of the pull-up means and a second end is connected to the output terminal, and a discharging means for forcibly discharging the capacitor depending on an external input control signal, the pull-up driving means turning on the pull-up means by charging the capacitor in response to the front edge of the input signal and turning off the pull-up means by forcibly discharging the capacitor in response to the front edge of the output signal of the next stage.

54. The shift register of claim 53, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which gate is connected to the input signal, drain is connected to a second power voltage and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage;

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is connected to the first power voltage; and

a fourth transistor of which drain is connected to the input node of the pull-up means, source is connected to the first power voltage and gate forcibly discharges the capacitor which receives the external input control signal.

55. The shift register of claim 54, wherein the external input control signal has a voltage level capable of turning on the fourth transistor when a power is applied and turning off the fourth transistor before the start signal is applied to the first stage.

56. The shift register of claim 55, wherein the external input control signal has a voltage level capable of turning off the fourth transistor while the start signal is applied to the first stage and an output of a last shift register is generated, and turning on the fourth transistor after the output of the last shift register is generated, thereby discharging the capacitor of the last shift register.

57. The shift register of claim 53, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which gate is connected to the input signal, drain is connected to a second power voltage and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source receives the external input control signal to forcibly discharge the capacitor.

58. The shift register of claim 57, wherein the sources of the second transistor and the third transistor are commonly connected to each other.

59. The shift register of claim 57, wherein the external input control signal maintains a low state simultaneously with an application of a power to thereby forcibly discharge the capacitor, and maintains a high state before the start signal applied to the first stage is generated.

60. The shift register of claim 58, wherein the external input control signal maintains a low state simultaneously with an application of a power to thereby forcibly discharge the capacitor, and maintains a high state before the start signal applied to the first stage is generated.

61. The shift register of claim 59, wherein the external input control signal has a voltage level capable of turning on the third transistor when a power is applied, and turning off the third transistor before the start signal is applied to the first stage.

62. The shift register of claim 61, wherein the turning on voltage level is the second power voltage, and the turning off voltage level is the first power voltage.

63. The shift register of claim 57, wherein the second power voltage is above a threshold voltage capable of turning on the third transistor even when the first power voltage is applied to the gate terminal of the third transistor and less than the first power voltage.

64. The shift register of claim 63, wherein the external input control signal has a voltage level capable of turning off the third transistor while the start signal is applied to the first stage and an output of a last shift register is generated, and turning on the third transistor after the output of the last shift register is generated, thereby discharging the capacitor of the last shift register.

65. An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages connected in cascade fashion, the multiple stages having a first stage in which a start signal is coupled to an input terminal, the shift register for sequentially selecting the multiple gate lines depending on output signals of the respective stages, the multiple stages having odd stages for receiving a first clock signal, and even stages for receiving a second clock signal having a phase opposite to the first clock signal,

wherein each of the multiple stages comprises:

an input terminal connected to an output terminal of a previous stage;

an output terminal connected to a corresponding gate line;

a control terminal connected to a control terminal of a next stage;

a clock terminal into which a corresponding clock signal is inputted;

an external input control terminal for receiving an external input control signal;

a pull-up means for providing a corresponding one out of the first and second clock signals to the output terminal;

a pull-down means for providing a first power voltage to the output terminal;

a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to a front edge of the input signal and turning on the pull-down means in response to a front edge of an output signal of a next stage; and

a pull-up driving means provided with a capacitor of which one end is connected to an input node of the pull-up means and the other end is connected to the output terminal, and a discharging means for forcibly discharging the capacitor depending on the external input control signal applied to the external input control terminal, the pull-up driving means turning on the pull-up means by charging the capacitor in response to the front edge of the input signal and turning off the pull-up means by forcibly discharging the capacitor in response to the front edge of the output signal of the next stage.

66. The LCD of claim 65, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which gate is connected to the input signal, drain is connected to a second power voltage and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the

pull-up means, gate is connected to the input node of the pull-down means and source is connected to the input node of the pull-up means;

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source is connected to the first power voltage; and

a fourth transistor of which drain is connected to the input node of the pull-up means, source is connected to the first power voltage and gate forcibly discharges the capacitor which receives the external input control signal.

67. The LCD of claim 66, wherein the external input control signal has a voltage level capable of turning on the fourth transistor when a power is applied and turning off the fourth transistor before the start signal is applied to the first stage.

68. The LCD of claim 67, wherein the external input control signal has a voltage level capable of turning off the fourth transistor while the start signal is applied to the first stage and an output of a last shift register is generated, and turning on the fourth transistor after the output of the last shift register is generated, thereby discharging the capacitor of the last shift register.

69. The LCD of claim 65, wherein the pull-up driving means comprises:

a capacitor connected between the input node of the pull-up means and the output terminal;

a first transistor of which gate is connected to the input signal, drain is connected to a second power voltage and source is connected to the input node of the pull-up means;

a second transistor of which drain is connected to the input node of the pull-up means, gate is connected to the input node of the pull-down means and source is connected to the first power voltage; and

a third transistor of which drain is connected to the input node of the pull-up means, gate is connected to the output signal of the next stage and source receives the external input control signal to forcibly discharge the capacitor.

70. The LCD of claim 69, wherein the sources of the second transistor and the third transistor are commonly connected to each other.

71. The LCD of claim 69, wherein the external input control signal maintains a low state simultaneously with an application of a power to thereby forcibly discharge the capacitor, and maintains a high state before the start signal applied to the first stage is generated.

72. The LCD of claim 70, wherein the external input control signal maintains a low state simultaneously with an application of a power to thereby forcibly discharge the capacitor, and maintains a high state before the start signal applied to the first stage is generated.

73. The LCD of claim 70, wherein the external input control signal has a voltage level capable of turning on the third transistor when a power is applied and turning off the third transistor before the start signal is applied to the first stage.

74. The LCD of claim 73, wherein the turning on level is the second

power voltage level and the turning off voltage level is the first power voltage level.

75. The LCD of claim 70, wherein the second power voltage is above a threshold voltage capable of turning on the third transistor even when the first power voltage is applied to the gate terminal of the third transistor and less than the first power voltage.

76. The LCD of claim 75, wherein the external input control signal has a voltage level capable of turning off the third transistor while the start signal is applied to the first stage and an output of a last shift register is generated, and turning on the third transistor after the output of the last shift register is generated, thereby discharging the capacitor of the last shift register.